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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	9

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,923	KEMENY, JOHN	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31* is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to Amendment A filed on 01/20/2004, paper #8. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The rejection of claims 1-30 under 35 U.S.C. 102(e) as being anticipated by Van Hook et al., U.S. Patent 6549210 B1 are maintained as shown below.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al., U.S. Patent 6549210 B1.

Regarding claims 1 and 17, Van Hook teaches that a method of data storage address translation, the method comprising:

receiving a first address (Fig.9, DRAM address or addresses of the Tile) in a first address space (DRAM 900);

traversing a trie (it is taught as the tiles with the DRAM as shown in Fig.9) based on the first address (Fig.9, col.15, lines 60 to col.16, lines 12); and

determining a second address (cache addresses such as cache lines) based on the traversal (col.16, lines 5-9).

Regarding claims 2 and 18, Van Hook teaches that the first address has a different address space than the second address (it is taught as DRAM 900 has the address space as shown in Fig.9 different than the cache memory 901).

Regarding claims 3 and 19, Van Hook teaches that the first address has a larger address space than the second address (col.13, lines 51-67).

Regarding claims 4 and 20, Van Hook teaches that the trie includes at least one leaf (Tile0 through Tile 6) identifying an address (cache addresses 0 through C-1) in the second address space (cache memory 901).

Regarding claims 5 and 21, Van Hook teaches that the second address comprises an address of a cache memory (cache 901 as shown in Fig.9 having addressable cache lines).

Regarding claims 6,13 and 22, Van Hook teaches further comprising, based on the traversal, determining whether the cache stores information identified by the first address (it is taught as cache hit or cache miss in col.16, lines 66 to col.17, lines 22).

Regarding claims 7 and 23, Van Hook teaches that the trie comprises a multi-dimensional array (col.2, lines 17-30), wherein an index of a dimension of the array corresponds to different trie branches (col.18, lines 19-45).

Regarding claim 8, Van Hook teaches that traversing the trie comprises, repeatedly, indexing into the dimension of the array using a portion of the first address (col.17, lines 62 to col.18, lines 18).

Regarding claims 9 and 24, Van Hook teaches that the first address comprises an address of permanent data storage (the addresses of DRAM is the addresses of permanent data storage).

Regarding claims 10,15 and 25, Van Hook teaches that traversing the trie based on the first address comprises performing an operation on the first address (it is taught

as calculating the memory location in DRAM for the texel, col.15, last line to col.16, lines 5); and traversing the trie using the operation results (it is taught as loading a cache line by accessing the DRAM addresses M0 through M0+(k-1)).

Regarding claims 11,16 and 26, Van Hook teaches that the second address associated with the first address dynamically changes (col.15, lines 60 to col.16, lines 12).

Regarding claim 12, Van Hook teaches that a data storage system, comprising:

(a) a storage area having a first address space (Fig.9, DRAM 900);

(b) a cache having a second address space (Fig.9, cache 901); and

(c) instructions for causing a processor (Fig.9, texel processing 904) to

(1) receive a first address (Fig.9, DRAM address or addresses of the tile) in the first address space (DRAM 900);

(2) traverse a trie based on the first address (Fig.9, col.15, lines 60 to col.16, lines 12); and

(3) determine a second address (cache addresses such as cache lines) in the second address space (Fig.9, cache memory 901) based on the traversal (col.16, lines 5-9).

Regarding claim 14, Van Hook teaches that the instructions for causing the processor to receive a first address comprise instructions for causing the processor

(Fig.9, texel processing 904) to receive a first address included in a data access request received from a host (it is taught as texel requests from texel processing component 904) connected to the data storage system (DRAM storage system).

Regarding claim 27, Van Hook teaches that a method of data storage address translation at a system having a storage area composed of different physical devices (DRAM storage device 900 as shown in Fig.9), a shared cache (cache memory 901) for caching blocks of data in the storage area, and connections to different host processors, the method comprising:

receiving a storage area address within a storage area address space based on a request received from one of the host processors (it is taught as texel requests from texel processing component 904);

traversing a trie based on the storage area address (Fig.9, col.15, lines 60 to col.16, lines 12), the traversing identifying a trie leaf (it is taught as the tiles Tile0 through Tile 6 within the DRAM as shown in Fig.9) identifying a cache address in a cache address space (cache addresses 0 through C-1); and

changing the cache address associated with the trie leaf based on system alteration of cache contents (col.15, lines 60 to col.16, lines 12).

Regarding claim 28, Van Hook teaches that a memory (Fig.9, DRAM memory 900) for storing data for access by an application program being executed on a data processing system (Fig.9, texel processing 904), comprising a data structure (it is taught

as a texture image comprising a texel array, col.4, lines 27-32 and lines 46-48) stored in said memory (texel image DRAM), said data structure including information (it is taught as image data i.e. textels within DRAM) corresponding to a trie (it is taught as the tiles within the DRAM as shown in Fig.9), the trie having leaves (Tile0 through Tile 6) identifying different respective cache addresses (cache addresses 0 through C-1).

Regarding claim 29, Van Hook teaches that the trie comprises a trie having branches corresponding to different portions of a storage area address (it is taught as the tiles with the DRAM as shown in Fig.9).

Regarding claim 30, Van Hook teaches that the trie comprises a multi-dimensional array (col.2, lines 17-30).

Allowable Subject Matter

6. Claim 31 is allowed.

Response to applicant's Arguments

7. Applicant's arguments filed 01/20/2004 regarding independent claims have been fully considered but they are not persuasive.

In response to the applicant's argument that Van Hook does not refer to a trie data structure that is traversed based on a first address to determine a second address, and a tag table as described in the Van Hook is not the same as or equivalent to a trie data structure (third paragraph, lines 8-12 of the applicant's response), applicant must

discuss the references applied against the claims, explaining how the claims avoid the references or distinguish from them, however, the arguments of the third paragraph, lines 8-12 of the applicant's response has only generic statement regarding the reference without specifically addressing the points set-forth in the Examiner's rejection. In addition, the Examiner believes that "traversing the trie may include performing an operation on the first address and traversing the trie using the operation results" (according to the applicant's specification page 2, second paragraph) is taught as a tag table in Van Hook is traversed to locate a cache address based on a DRAM address. Therefore, the tag table is equivalent to a trie and the limitations in the independent claims are taught in the Van Hook.

8. In response to the applicant's argument that Van Hook hashes a cache index to avoid cache aliasing and uses this hashed index to improve upon the efficiency of the cache rather than improve upon the efficiency of cache indexing itself of the presently-claimed invention (third paragraph, lines 13-21 of the applicant's response), it is noted that the features upon which applicant relies (i.e., the use of a trie data structure and its traversal to identify related cache addresses provide significant performance advantage) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Mano Padmanabha
4/4/04

Jasmine Song
Patent Examiner
April 4, 2004

Mano Padmanabhan
Supervisory Patent Examiner
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